REMARKS

The present response is intended to be fully responsive to all points of objection and/or rejection raised by the Examiner and is believed to place the application in condition for allowance. Favorable reconsideration and allowance of the application is respectfully requested.

Applicant asserts that the present invention is new, non-obvious and useful. Prompt consideration and allowance of the claims is respectfully requested.

Status of Claims

Claims **1-35** are pending in the application.

Claims **1-35** have been rejected.

CLAIM REJECTIONS

35 U.S.C. § 103 Rejections

In the Office Action, the Examiner rejected claims 1-35 under 35 U.S.C. § 103(a), as being unpatentable over Bujanos (U.S. Pat. No. 5,572,664) in view of Brown III et al. (U.S. Pat. No. 5,450,555).

Applicant respectfully traverses this rejection. Applicant asserts that neither Bujanos nor Brown III et el., alone or in cousin, teach or suggest, and the Examiner does not assert that Bujanos or Brown III et al. teach or suggest

"a receiver for receiving a list of floating-point commands in a formal computer language; the language having set based constraints that facilitate defining Floating-Point events of interest in respect of at least one FP instruction", as recited in independent claim **1**. It would not have been obvious and the Examiner does not suggest that it would have been obvious, to include "receiving a list of floating-point commands in a formal computer language" and "the language having set based constraints that facilitate defining Floating-Point events of interest in respect to at least one FP instruction" in Bujanos or in Brown III et al.

Bujanos describes a test-vector generating system that controls a processor having a paradigm floating point functional unit which executes a paradigm floating point instruction set (abstract). As Examiner Kendall correctly states, Bujanos does not disclose receiving a list of floating point commands, Bujanos does disclose a floating point unit which executes <u>floating point command sets</u>.

Brown III et al. describes a pipelined processor with an instruction unit for decoding instructions and pre-processing operands prior to instruction execution, and an execution unit for executing the decoded instructions (abstract). Brown III et al. describes a solution to a problem relevant <u>to complex instruction sets or CISC type processors</u>

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(Col.1, lines 36-37). The floating point processor mentioned by Brown is an execution unit for <u>floating point and integer multiply instructions</u> (Col. 8, lines 9-11). More specifically, Brown III et al. describes executing specific floating point commands (adds, multiplies and divides) by the floating point unit (Col. 11, lines 34-37). Even if the Examiner's statement that combining Bujanos and Brown would have been obvious to one of ordinary skill in the art because it would enable the floating point unit to be able to execute a wider range of floating point commands, is accepted, Applicant respectfully asserts that neither Bujanos nor Brown III et al. teach or suggest "receiving a list of floating-point commands in a formal computer language" and "the language having set based constraints that facilitate defining Floating-Point events of interest in respect to at least one FP instruction", as recited in claim 1 of the present invention.

Thus, neither Bujanos nor Brown et al., alone or in combination, teach or suggest the invention of claim 1. Similarly, Applicant respectfully traverses the rejection to independent claims 8, 13, and 27-35. In regard to these claims, the Examiner cited the same passages of Bujanos and Brown III et al. None of the cited passages, however, disclose or suggest "a formal computer language… having set based

constraints that facilitate defining Floating-Point events of interest" as recited in claims **8, 13,** and **27-35.**

Claims **2-7, 9-12,** and **14-26** depend from, directly or indirectly, claims **1, 8, 13,** and **27-35,** and therefore include all the elements of those claims. Therefore, Applicant respectfully asserts that claims **2-7, 9-12,** and **14-26** are likewise allowable. Accordingly, Applicant respectfully requests that the Examiner withdraw the rejections to independent claims **1, 8, 13,** and **27-35** and to claims **2-7, 9-12,** and **14-26** dependent thereon.

Applicant believes the remarks presented hereinabove to be fully responsive to all of the grounds of rejection raised by the Examiner. In view of these remarks, Applicant respectfully submits that all of the claims in the present application are in order for allowance. Notice to this effect is hereby requested.

If the Examiner has any questions he is invited to contact the undersigned at 202-628-5197.

Respectfully submitted,

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